OIPE JC158
APR 08 2004
PATENT & TRADEMARK OFFICE

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 10/797,443
	Filing Date: March 9, 2004
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventor: Jason Wei
"SYSTEM AND METHOD FOR SELECTING OPTIMAL DATA TRANSITION TYPES FOR CLOCK AND DATA RECOVERY"	Group Art Unit: Unknown
	Examiner Name: Unknown
	Attorney Docket No.: RA327.P.US

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A						
	B						
	C						
	D						

Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	E							

OTHER ART (Including Author, Title, Date, Pertinent Pages; Etc.)

/K.K./	F	MARTIN, Aaron et al., "8 Gb/s Differential Simultaneous Bidirectional Link with 4mV 9ps Waveform Capture Diagnostic Capability." September 2003, IEEE International Solid-State Circuits Conference. Session 4/Clock Recovery and Backplane Transceivers/paper 4.5. 10 pages.
/K.K./	G	KASTURIA, Sanjay and WINTERS, Jack H., "Techniques for High-Speed Implementation of Nonlinear Cancellation." June 1991, IEEE Journal on Selected Areas in Communications Vol. 9. No. 5. Pages 711-717.
/K.K./	H	WINTERS, Jack H. and KASTURIA, Sanjay, "Adaptive Nonlinear Cancellation for High-Speed Fiber-Optic Systems." July 1992, IEEE Journal of Lightweight Technology, Vol. 10, No. 7. Pages 971-977.
/K.K./	I	PARHI, Keshab K., "Pipelining in Algorithms with Quantizer Loops." July 1991. IEEE Transactions on Circuits and Systems, Vol. 38, No. 7. Pages 745-754.
/K.K./	J	PARHI, Keshab K., "High-Speed Architectures for Algorithms with Quantizer Loops." August 1990. Proc. ISCAS. Pages 2357-2360.

Examiner /Kevin Kim/	Date Considered 04/11/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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/K.K./	G	Stojanovi, Vladimir et al. "Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver." Rambus, Inc. Department of Electrical Engineering, Stanford University. January 2004. 4 pages.
/K.K./	H	Zerbe, J. et al. "Equalization and Clock Recovery for a 2.5 - 10Gbs 2-PAM/4-PAM Backplane Transceiver Cell." Presented at ISSCC 2003, paper 4.6. 2 pages.
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	K	

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